IN THE CLAIMS

Please amend the following claims which are pending in the present application:

1. (Previously presented) A polymer memory, comprising:

a first plurality of conductive word lines extending parallel to one another in a y-direction and having center lines spaced from one another by a first distance in an x-direction;

a first ferroelectric polymer memory material in x- and y-directions over the word lines; and

a plurality of conductive bit lines extending parallel to one another in the x-direction over the first ferroelectric polymer memory material and having center lines spaced from one another by a second distance in the y-direction, the second distance being less than the first distance, a first array of polymer memory cells being defined in the first ferroelectric polymer memory material, each where a respective bit line crosses over a respective one of the first plurality of word lines, such that the ferroelectric polymer memory material at a respective cell of the first array is changed when a select voltage difference is applied over respective word and bit lines on opposing sides of the respective cell.

2. (Original) The polymer memory of claim 1, further comprising:

a second ferroelectric polymer memory material in x- and y-directions over the bit lines; and

a second plurality of conductive word lines extending parallel to one another in the y-direction over the second ferroelectric polymer memory material and having center lines spaced from one another by a third distance, equal to the first distance, in the x-direction, a second array of polymer memory cells being defined in the second ferroelectric polymer memory material, each where a respective one of the second plurality of word lines crosses over a respective bit line, such that the ferroelectric polymer memory material at a respective cell of the respective second array is changed when a select voltage difference is applied over respective bit and word lines opposing the respective cell.

3. (Original) The polymer memory of claim 2, wherein each word line has a first width in the x-direction and each bit line has a second width in the y-direction, the second width being less than the first width.

4. (Original) The polymer memory of claim 3, wherein adjacent ones of the word lines are spaced from one another by a first spacing in the x-direction, and adjacent ones of the bit lines are spaced from one another by a second spacing in the y-direction, the first spacing being more than the second spacing.

5. (Currently amended) A polymer memory, comprising:

a plurality of multi-layer constructions, each including a plurality of bit lines extending parallel to one another in an x-direction and having center lines spaced

from one another by a first distance in a y-direction, ferroelectric polymer memory material on first and second opposing sides of the bit lines, and first and second pluralities of conductive word lines with the ferroelectric polymer memory material and bit lines between the first and second pluralities of word lines, the word lines of each plurality extending parallel to one another in the y-direction and having center lines spaced from one another by a second distance in the x-direction, the second distance being more than the first distance, a first array of polymer memory cells being defined in the ~~first~~ ferroelectric polymer memory material on the first side of the bit lines, each where a respective bit line crosses over a respective one of the first plurality of word lines, such that the ferroelectric polymer memory material at a respective cell of the first array is changed when a select voltage difference is applied over respective word and bit lines on opposing sides of the respective cell, a second array of polymer memory cells being defined in the ~~second~~ ferroelectric polymer memory material on the second side of the bit lines, each where a respective bit line crosses over a respective one of the second plurality of word lines, such that the ferroelectric polymer memory material at a respective cell of the second array is changed when a select voltage difference is applied over respective word and bit lines on opposing sides of the respective cell; and

a plurality of insulating layers, each between a respective pair of the multi-layer constructions.

6. (Original) The polymer memory of claim 5, wherein each word line has a first width in the x-direction and each bit line has a second width in the y-direction, the second width being less than the first width.

7. (Original) The polymer memory of claim 6, where adjacent ones of the word lines are spaced from one another by a first spacing in the x-direction and adjacent ones of the bit lines are spaced from one another by a second spacing in the y-direction, the first spacing being more than the second spacing.

8. (Original) A polymer memory, comprising alternating layers of conductive lines and ferroelectric polymer memory material, some of the layers of conductive lines having word lines extending in a y-direction and other ones of the layers of conductive lines having bit lines extending in an x-direction, the conductive lines of some of the layers having center lines spaced by a first distance and conductive lines of other ones of the layers having center lines spaced by a second distance which is less than the first distance.

9. (Original) The polymer memory of claim 8, wherein the layers with conductive lines having center lines spaced by the second distance comprise less than 50% of the layers of conductive lines.

10. (Original) The polymer memory of claim 9, wherein the layers with

conductive lines having center lines spaced by the second distance comprise less than 30% of the layers of conductive lines.

11-15. (Cancelled)